GigaDevice Semiconductor Inc.

GD32E103/C103 系列移植到 GD32F30x 系列

应用笔记

AN047

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1. 前言

本应用笔记旨在帮助您快速将应用程序从 GD32E103/C103 系列控制器移植到 GD32F30x 系列控制器。

为了更好的利用本应用笔记中的信息，您需要从官网 www.GD32MCU.com 下载 GD32 各系列微控制器资料，如 Datasheet、用户手册、官方例程及各种开发工具等。

2. 引脚兼容性

GD32F30x 与 GD32E103/C103xx 在相同封装下是 Pin To Pin 兼容的。但由于 GD32E103xx 没有 CAN 外设，故引脚上有细微的功能差别，这里以 GD32F303/F305/F307xx 为例。

GD32F303xx、GD32F305/F307xx 和 GD32E103/C103xx 引脚区别详细说明见*表 2-1. 引脚对比*。

表 2-1. 引脚对比

引脚号	GD32F303xx引脚定义	GD32F305/F307xx引脚定义	GD32E103/C103xx引脚定义
PF0	Default: PF0 Alternate: EXMC_A0 Remap: CTC_SYNC	Default: PF0 Alternate: EXMC_A0 Remap: CTC_SYNC	GD32E103/C103xx没有144Pin封装，不存在PF0引脚
PB5	Default: PB5 Alternate: I2C0_SMBA, SPI2_MOSI, I2S2_SD Remap: TIMER2_CH1, SPI0_MOSI	Default: PB5 Alternate: I2C0_SMBA, SPI2_MOSI, I2S2_SD Remap: TIMER2_CH1, SPI0_MOSI, CAN1_RX	Default: PB5 Alternate: I2C0_SMBA, SPI2_MOSI, I2S2_SD Remap: TIMER2_CH1, SPI0_MOSI, CAN1_RX
PB6	Default: PB6 Alternate: I2C0_SCL, TIMER3_CH0 Remap: USART0_TX, SPI0_IO2	Default: PB6 Alternate: I2C0_SCL, TIMER3_CH0 Remap: USART0_TX, CAN1_TX, SPI0_IO2	Default: PB6 Alternate: I2C0_SCL, TIMER3_CH0 Remap: USART0_TX, CAN1_TX, SPI0_IO2
PB12	Default: PB12 Alternate: SPI1_NSS, I2C1_SMBA, USART2_CK, TIMER0_BRKIN, I2S1_WS	Default: PB12 Alternate: SPI1_NSS, I2C1_SMBA, USART2_CK, TIMER0_BKIN, I2S1_WS, CAN1_RX	Default: PB12 Alternate: SPI1_NSS, I2S1_WS, I2C1_SMBA, USART2_CK, TIMER0_BRKIN, CAN1_RX
PB13	Default: PB13 Alternate: SPI1_SCK, USART2_CTS, TIMER0_CH0_ON, I2S1_CK	Default: PB13 Alternate: SPI1_SCK, USART2_CTS, TIMER0_CH0_ON, I2S1_CK, CAN1_TX	Default: PB13 Alternate: SPI1_SCK, I2S1_CK, USART2_CTS, TIMER0_CH0_ON, CAN1_TX, I2C1_TXFRAME

注：

1. GD32F305xx、GD32F307xx 都有 2 路 CAN，GD32F303xx 只有一路 CAN。
2. GD32E103xx 的 TMIER8_CH0/TMIER8_CH1/TMIER12_CH0 只在 GD32F30xVG/I/K 上有此功能。

3. 内部资源兼容性

下表给出了 GD32F30x 与 GD32E103/C103xx 的资源对比(以 GD32F303xx,GD32F305xx 和 GD32E103/C103xx 对比为例)，详细说明见*表 3-1. 资源对比*。

表 3-1. 资源对比

片内资源	GD32F303xx	GD32F305xx	GD32E103/C103xx	兼容性说明
主频	108MHz	120MHz	120MHz	主频存在差异
内核	M4内核	M4内核	M4内核	完全兼容
供电范围	2.6V-3.6V	2.6V-3.6V	1.8V-3.6V	GD32F30x的供电范围相对较窄
Flash	256-3072KB	128-1024KB	64-128K	Flash操作方式存在差异
RAM	48-96KB	64-96K	32K	
GPTM	4/10	4/10	4/10	兼容对应芯片存在的外设
Advanced TM	1/2	1/2	1/2	兼容对应芯片存在的外设
Basic TM	2	2	2	完全兼容
Systick	1	1	1	完全兼容
Watch dog	2	2	2	完全兼容
RTC	1	1	1	完全兼容
U(S)ART	3/5	5	2/3/5	兼容对应芯片存在的外设
I2C	2	2	1/2	兼容对应芯片存在的外设
SPI/IIS	3/2	3/2	1-3/2	兼容对应芯片存在的外设
CAN	1	2	0/2	GD32F303/F305xx只支持CAN2.0
USBFS	1(USBD)	1(USBOTG)	1(USBOTG)	GD32F303xx属于USBD，GD32F305xx和GD32E103/C103xx兼容
GPIO	37/51/80112	51/80/112	26/37/51/80	兼容对应芯片存在的外设
EXMC	0/1	0/1	0/1	100pin封装的GD32F305xx和GD32E103/C103xx都有一个EXMC，GD32F305xx新增了EXMC部分功能
ADC(CH)	3(16/21)	2（16）	2（10/16）	兼容对应芯片存在的外设
DAC	2	2	2	完全兼容
CTC	1	1	1	完全兼容

注：

1. GD32F305xx、GD32F307xx 都有 2 路 CAN，GD32F303xx 只有一路 CAN。
2. GD32E103xx 的 TMIER8_CH0/TMIER8_CH1/TMIER12_CH0 只在 GD32F30xVG/I/K 上有此功能。

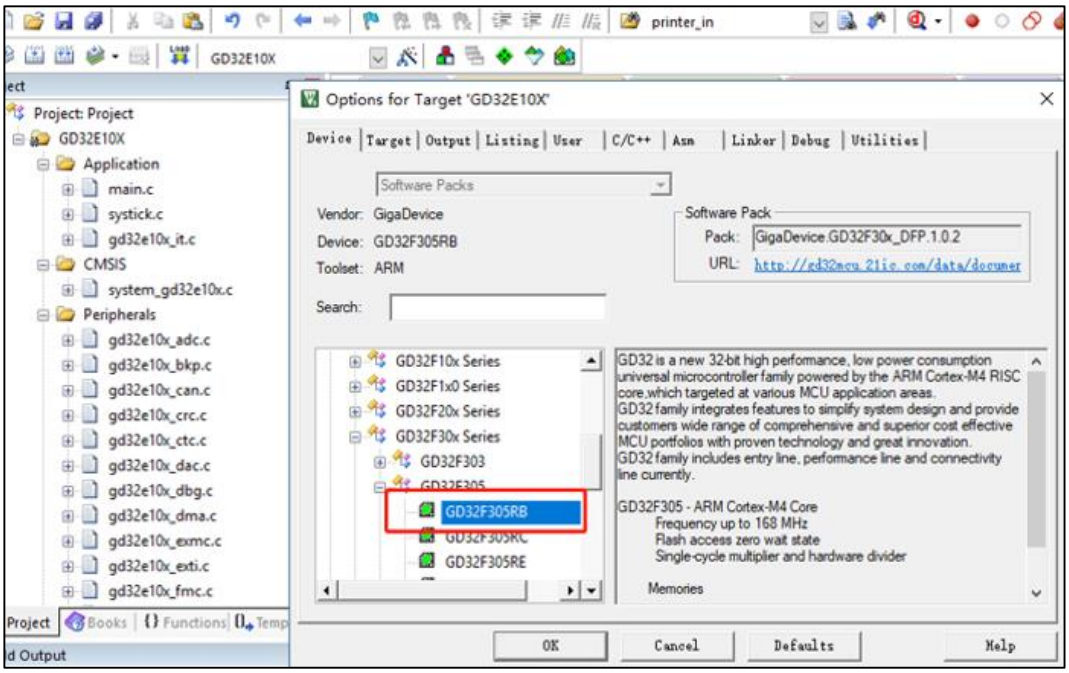
4. 程序移植

GD32E103/C103xx 外设上和时钟与 GD32F30x 互联系列基本兼容，在基于 GD32E103/C103xx 固件库应用程序移植到 GD32F30x 上也需要做部分修改和调整。

4.1. IDE 设置

1. 使用 MDK 环境时，安装 GD32F30x 系列插件，更换为 GD32F30x 对应的型号(此处以移植到 GD32F305RB 为例)。

图 4-1. 修改设备型号



2. 使用 IAR 环境时，在工程中也同样更换设备型号。

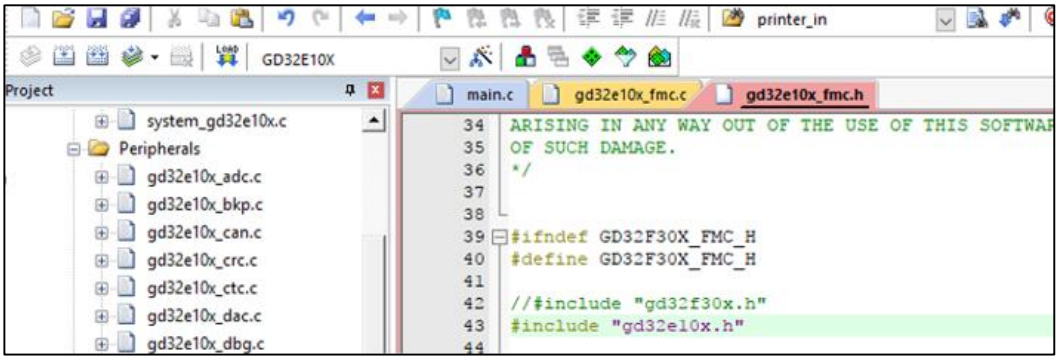
4.2. FMC 外设文替换

GD32E103/C103xx 采用的嵌入式 E-Flash 架构。GD32E103/C103xx 的 flash 编程上支持的是整字、半字编程。

GD32F30x 采用的 SIP 叠封架构，flash 编程上也支持整字，半字编程，且有 bank0、bank1 的划分，对于选项字节的操作也需要按字进行编程。

建议采用便捷的移植方法:将原工程中的 gd32e10x_fmc.c 和 gd32e10x_fmc.h 中的代码替换为 GD32F30x 固件库中的 gd32f30x_fmc.c 和 gd32f30x_fmc.h 内的代码，替换后需要再把所有相关的#include"gd32e10x.h"更改为#include"gd32f30x.h"即可，详见*图 4-2. 替换代码后修改头文件*。GD32E103xx 固件库可从官网或网盘中获取。

图 4-2. 替换代码后修改头文件

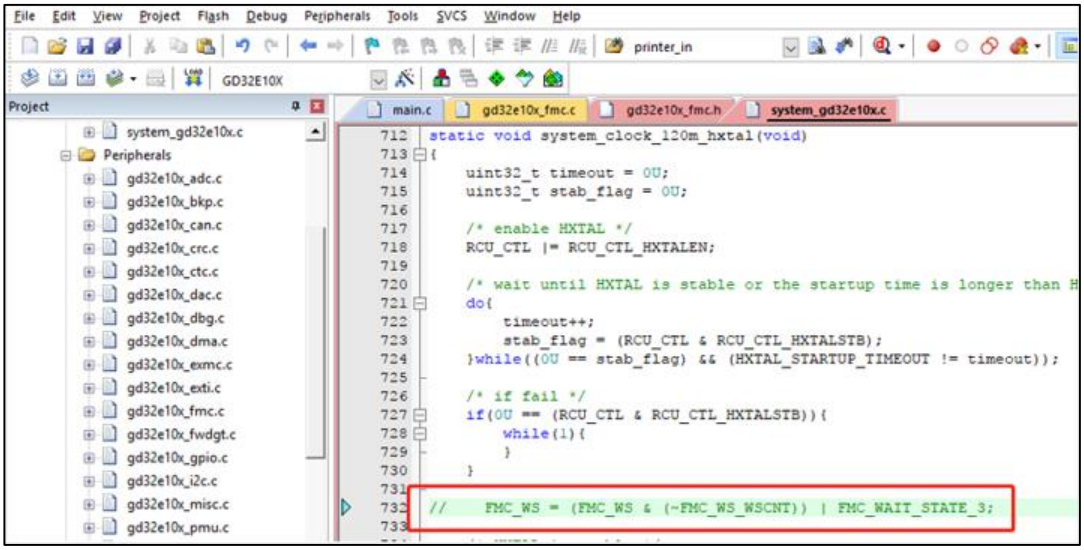


4.3. 系统时钟配置

GD32F30x 互联型系列和 GD32E103/C103xx 的时钟配置过程相同，GD32E103/C103xx 上有 Flash 等待周期，需要在时钟配置前加入相应的 Flash 等待周期, 但对于 GD32F30x 系列只分为 code 区和 data 区，code 区均为零等待区域，故不需要对 flash 插入任何等待周期

在 system_gd32f30x.c 文件中的时钟配置函数里去除 Flash 等待周期的配置，见*图 4-3. 去除等待周期*所示。

图 4-3. 去除等待周期



注： 如果使用 GD32F303xx 进行替换，建议更换 system_gd32e10x.c 文件，操作方式参考 FMC 的替换方式。

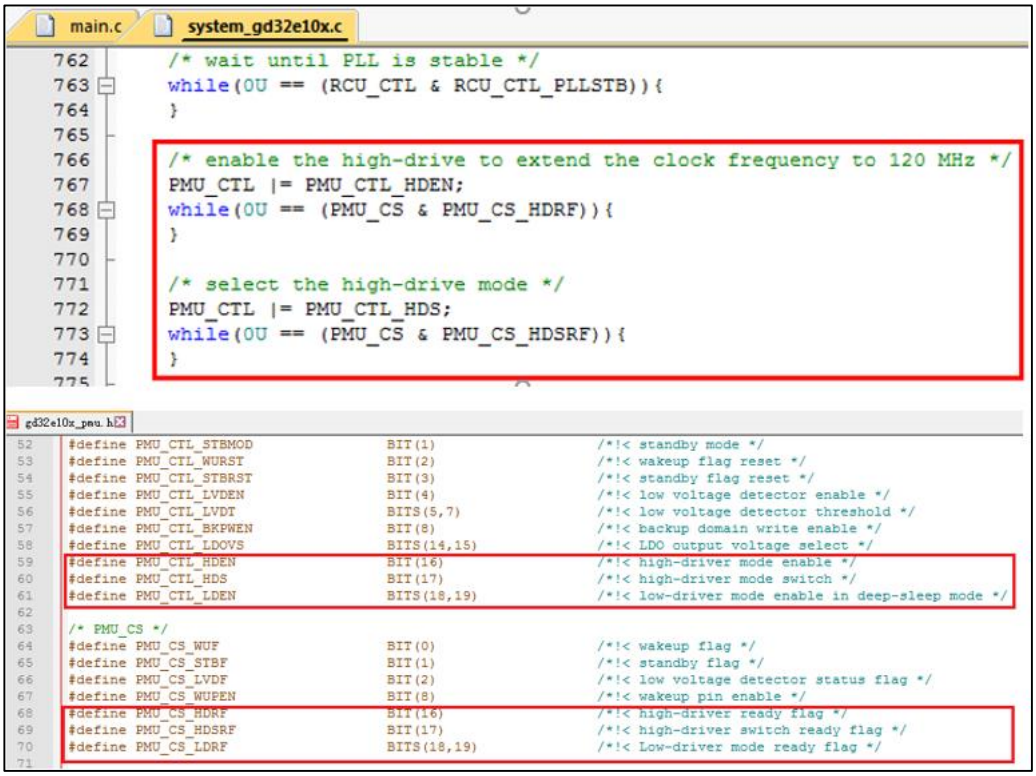
5. 外设差异性

GD32F30x 与 GD32E103/C103xx 在外设上大部分兼容的。

5.1. 电源管理单元（PMU）

GD32F30x PMU 模块新增了高驱模式，如有需要需手动自己定义。见*图 5-1. 新增高驱模式*所示。

图 5-1. 新增高驱模式



另外，功耗方面 GD32F30x 相较 GD32E103/C103xx 在同一个模式下功耗会相对偏高，具体可以参考数据手册。

5.2. 控制局域网络（CAN）

1. GD32C103xx 的 CAN 是 CAN FD，而 GD32F30x 的 CAN 是普通 CAN2.0B，不支持 CAN FD，通信波特率最大为 1Mbit/s，在非互联型 GD32F30x 系列产品中有 14 个过滤器；在互联型 GD32F30x（CL）系列产品中有 28 个过滤器。
2. CAN 外设固件驱动参考上文 FMC 的移植方式进行修改。

注： GD32F303xx 为 USBD 与 CAN 共享 512 字节的专用 SRAM 用于数据缓冲，故不能同时使用。

5.3. 外部存储器控制器（EXMC）

GD32F30x 的 EXMC 相比 GD32E103/C103xx 多了 8 位或 16 位的 NAND Flash 以及 16 位的 PC Card 控制器，且每个 BANK 都有独立的信号。

5.4. 通用串行总线全速接口（USBD/USBFS）

GD32E103xx 和 GD32F305/F307xx 的 USBFS 基本一致，GD32F303xx 为 USBD 与 CAN 共享 512 字节的专用 SRAM 用于数据缓冲，不能同时使用。GD32F305/F307xx 为 USBOTG 有单独的 USBSRAM，不存在不能共用的问题。

6. 移植注意事项

6.1. 软件延时调整

GD32E103xx 的 Flash 运行有等待周期，GD32F30x 系列 Flash 为零等待设计，所以在同主频下效率 GD32F30x 会略高于 GD32E103/C103xx。如果用户代码有用到 for 循环或者是 while 循环语句来做延时，延时时间在 GD32F30x 系列上会变短，需要适当的增加延时参数或改用 Timer 来做延时函数，在使用 GPIO 模拟通信协议的应用场景下需特别注意。

6.2. Flash 编程

在 flash 擦除和编程时间上 GD32F30x 比 GD32E103xx 长，见*表 6-1. GD32F30x Flash 特性*以及

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max(2)	Unit
PECYC	Number of guaranteed program /erase cycles before failure (Endurance)	TA = -40 °C ~ +85 °C	100	—	—	kcycles
tRET	Data retention time	—	—	20	—	years
tPROG	Word programming time	TA = -40°C ~ +85 °C	—	37.5	86	µs
tERASE	Page erase time	TA = -40°C ~ +85 °C	—	45	200/300(3)	ms
tMERASE(256K)	Mass erase time	TA = -40°C ~ +85 °C	—	1	4.8/8.0(4)	s
tMERASE(512K)	Mass erase time	TA = -40°C ~ +85 °C	—	4	19.2/32(5)	s
tMERASE(1MB)	Mass erase time	TA = -40°C ~ +85 °C	—	6	28.8/48(6)	s
tMERASE(2MB)	Mass erase time	TA = -40°C ~ +85 °C	—	10	48/80(7)	s
tMERASE(3MB)	Mass erase time	TA = -40°C ~ +85 °C	—	14	67.2/112(8)	s

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) Max value with <50K cycles is 200 ms and >50K & <100K cycles is 300 ms.
(4) Max value with <50K cycles is 4.8 s and >50K & <100K cycles is 8.0 s.
(5) Max value with <50K cycles is 19.2 s and >50K & <100K cycles is 32 s.
(6) Max value with <50K cycles is 28.8 s and >50K & <100K cycles is 48 s.
(7) Max value with <50K cycles is 48 s and >50K & <100K cycles is 80 s.
(8) Max value with <50K cycles is 67.2 s and >50K & <100K cycles is 112 s.

表 6-2. GD32E103/C103xx Flash 特性所示。

表 6-1. GD32F30x Flash 特性

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max(2)	Unit
PE_{CYC}	Number of guaranteed	T_A = -40 °C ~ +85 °C	100	—	—	kcycles

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max(2)	Unit
	program /erase cycles before failure (Endurance)					
t_{RET}	Data retention time	—	—	20	—	years
t_{PROG}	Word programming time	T_A = -40°C ~ +85 °C	—	37.5	86	µs
t_{ERASE}	Page erase time	T_A = -40°C ~ +85 °C	—	45	200/300(3)	ms
$t_{MERASE(256K)}$	Mass erase time	T_A = -40°C ~ +85 °C	—	1	4.8/8.0(4)	s
$t_{MERASE(512K)}$	Mass erase time	T_A = -40°C ~ +85 °C	—	4	19.2/32(5)	s
$t_{MERASE(1MB)}$	Mass erase time	T_A = -40°C ~ +85 °C	—	6	28.8/48(6)	s
$t_{MERASE(2MB)}$	Mass erase time	T_A = -40°C ~ +85 °C	—	10	48/80(7)	s
$t_{MERASE(3MB)}$	Mass erase time	T_A = -40°C ~ +85 °C	—	14	67.2/112(8)	s

(9) Based on characterization, not tested in production.
(10) Guaranteed by design, not tested in production.
(11) Max value with <50K cycles is 200 ms and >50K & <100K cycles is 300 ms.
(12) Max value with <50K cycles is 4.8 s and >50K & <100K cycles is 8.0 s.
(13) Max value with <50K cycles is 19.2 s and >50K & <100K cycles is 32 s.
(14) Max value with <50K cycles is 28.8 s and >50K & <100K cycles is 48 s.
(15) Max value with <50K cycles is 48 s and >50K & <100K cycles is 80 s.
(16) Max value with <50K cycles is 67.2 s and >50K & <100K cycles is 112 s.

表 6-2. GD32E103/C103xx Flash 特性

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PE_{CYC}(1)	Number of guaranteed program /erase cycles before failure(Endurance)	T_A = -40 °C ~ +85 °C	100	—	—	kcycles
t_{RET}(1)	Data retention time	10k cycles at T_A = 85 °C	10	—	—	years
t_{PROG}(2)	Word(3) programming time	T_A = -40 °C ~ +85 °C	37	—	44	µs
t_{ERASE}(2)	Page erase time	T_A = -40 °C ~ +85 °C	3.2	—	4	ms
t_{MERASE}(2)	Mass erase time	T_A = -40 °C ~ +85 °C	8	—	10	ms

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) Word is 32 bits or 64 bits depend on PGW bit in FMC_WS register.

6.3. 启动时间

GD32F30x 上电启动时间比 GD32E103xx 长。见*表 6-3. GD32F30x 启动时间*以及*表 6-4. GD32E103/C103xx 启动时间*所示。

表 6-3. GD32F30x 启动时间

Symbol	Parameter	Conditions	Typ	Unit
$t_{start-up}$	Start-up time	Clock source from HXTAL	144	ms
		Clock source from IRC8M	144	

(1) Based on characterization, not tested in production.
(2) After power-up, the start-up time is the time between the rising edge of NRST high and the main function.
(3) PLL is off.

表 6-4. GD32E103/C103xx 启动时间

Symbol	Parameter	Conditions	Typ	Unit
$t_{start-up}$	Start-up time	Clock source from HXTAL	468	μs
		Clock source from IRC8M	86.8	

(1) Based on characterization, not tested in production.
(2) After power-up, the start-up time is the time between the rising edge of NRST high and the first I/O instruction conversion in SystemInit function.
(3) PLL is off.

7. 版本历史

表 7-1. 版本历史

版本号.	说明	日期
1.0	首次发布	2022 年 3 月 15 日

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