GigaDevice Semiconductor Inc.

Precautions for GD32H7xx BootLoader Operation

Application Notes
AN126

Version 1.0

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1. Foreword

BootLoader of GD32H7xx supports three types of communication interfaces, including Usart, DFU and SDIO. Different interfaces require different hardware support. There are three Usart interfaces, including Usart0 (PA9, PA10), Usart1 (PA2, PA3), and Usart2 (PB10, PB11). There is only one DFU interface, namely USB0 (USBHS0_DP, USBHS0_DM). There is only one SDIO interface, namely SDIO0 (PC12, PD2, PB13, PC9, PC10, PC11). Basic operations of these interfaces are not described in details in this document. You may refer to related manuals. This document mainly describes operations of some special option bytes in GD32H7xx to avoid the chip from being locked due to users' misoperation.

2. Option byte operation

Operations of option bytes of GD32H7xx are mainly achieved by modifying related register. Each register consists of two groups (EFT register and MDF register). Users can modify MDF register only. For details, please refer to ***GD32H737_757_759 User Manual.*** The following context describes option byte operations to be noted during BootLoader operation.

2.1. DCRP operation

DCRP area can be set in FMC_DCRPADDR_MDF, but takes effect only if the start address is smaller than the end address. The set area can expand, but can not contract. For details, please refer to ***GD32H737_757_759 User Manual.*** Users can reset new areas after clearing original areas according to certain operational procedures.

Procedures of clearing DCRP area:

1. First set EREN bit of DCRP as 1, and then set SPC as any value other than 0xAA and 0xCC; that is, set the chip to read protection status.
2. After step 1 comes into effect, remove read protection.

After the two steps above are done, DCRP area is cleared. Please pay attention to two points below:

1. EREN bit and SPC bit can be set simultaneously, or SPC bit can be set after EREN bit comes into effect.
2. Both DCRP area and EREN bit of DCRP are cleared while read protection is removed.

2.2. SCR operation

SCR operation is to set secure areas. Please be careful when setting secure areas. Access to a secure area will disable JTAG and SWD interfaces and stop users from entering BootLoader. But the codes in the secure area can be set at will. Therefore, users can write a section of codes in the program running in the secure area to leave the secure area and exit from safe mode.

SCR area can be set in FMC_SCRADDR_MDF, but takes effect only if the start address is smaller than the end address. The set area can't be modified at will. In safe mode, the area can be modified and the secure area can be expanded, reduced, or deleted at will. In non-safe mode, if users wish to modify the area, they must delete the secure area before modification.

SCR area can be set only after SCR is enabled. Otherwise, the area setting would fail. SCR enabling is mainly achieved by setting SCR bit of OBSTAT0_MDF register.

Notes:

1. Once SCR is enabled, MCU will be activated from the address set in BOOT_ADDR0, regardless of Boot pin status.
2. Enabled SCR can be connected to MCU through JTAG or SWD interface, but the application can't be debugged or downloaded in IDE.

After setting SCR bit, click "Apply" button on the host computer interface and wait until the setting comes into effect. Only after the setting comes into effect, users can set SCR area. At setting SCR area, if the area is valid, the host computer will pop up a window to alert risks. Below is an example of setting SCR area:

1. Prepare a bin file which is downloaded and runs at 0x8000000. The running program in bin file will leave from the SCR area at the end and enter BootLoader again.
2. Adjust MCU Boot pin to make it enter BootLoader mode.
3. Download the bin file to 0x8000000, and make sure not to check the "Jump to run the App program" option in the host computer.
4. Set SCR bit of FMC_OBSTAT0_MDF in option bytes as 1 and set BOOT_ADDR0 bit field of FMC_BTADDR_MDF register as 0x1FF0 so that MCU can still start from BootLoader after SCR is enabled.
5. Set start and end addresses of SCR area in FMC_SCRADDR_MDF register. Make sure that the two addresses must be correct. Otherwise, the chip will be locked.
6. Once SCR area is set, MCU will run in SCR area every time it is booted.

Next, the document will introduce how to delete secure area in non-safe mode.

1. First set EREN bit of SCR as 1, then set SPC as any value other than AA and CC; that is, set the chip to read protection.
2. After step 1 comes into effect, remove read protection.

After the two steps above are done, SCR area is cleared. During operation, please pay attention to two points below:

1. EREN bit and SPC bit can be set simultaneously, or SPC bit can be set after EREN bit comes into effect.
2. While removing read protection, EREN bit of DCRP will be set, which is required when clearing SCR area.
3. After clearing SCR area, both EREN bits of SCR and DCRP will be set. At this time, they should be cleared according to certain steps.

In non-safe mode, EREN bits of SCR and DCRP can only be cleared according to the following steps.

1. Set SPC as any value other than AA and CC; that is, set the chip to read protection.
2. After step 1 comes into effect, remove read protection.

2.3. Hybrid operation of SCR and DCRP

After DCRP area and SCR bit are set, SCR bit can not be cleared directly. At this time, SCR bit and other bits in the register where SCR bit is located can not be modified simultaneously, and all modifications do not work. The only way to clear SCR bit is to clear DCRP area first.

3. Efuse operation

Efuse can be operated with Bootloader, but once a byte of Efuse is rewritten from 0 to 1, it can not be recovered to 0, so the operation is stricter. Therefore, it is recommended not to modify Efuse at will. Below is a brief introduction to a special operation in BootLoader.

Setting VFIMG bit of EFUSE_MCU_RSV register will stop users from setting SCR area. Similarly, users cannot set VFIMG bit after setting SCR area. If users need to enable both functions at the same time, there will be certain conflicts. At this time, users should set both functions according to the following steps:

1. First set SCR bit in option byte.
2. Check VFIMG bit of FUSE_MCU_RSV register in Efuse in the host computer and click the "Apply" button.
3. Set valid SCR area, and VFIMG bit is properly set at the same time.

The above operation succeeds because VFIMG must be set with SCR area at the same time. But it has a drawback. If users separately set SCR bit and VFIMG bit only, VFIMG can not be set normally. Therefore, it is recommended not to set VFIMG bit if there is no request of setting SCR area.

4. SDIO interface

Precautions for option byte and Efuse operation described above also apply to SDIO interface of Bootloader. Please note that written option bytes and Efuse can usually take effect only if Bootloader is subject to soft reset. However, as SD card update is an offline operation, to complete option byte or sequential Efuse operation mentioned above, users should copy different upgrade files from PC (option byte and Efuse configuration are different) to SD card for many times.

5. USB interface

As PHY of USB interface of GD32H7xx needs to be powered individually, special attention is required for the power supply mode of PHY of USB interface. If the power supply mode of PHY of USB interface is incorrect, DFU will not be identified. For the power supply mode of PHY of USB interface, please refer to ***Precautions for the Use of USBHS of AN117 GD32H7xx Series.***

6. OSPI

USART interface of GD32H7xx BootLoader is able to write data to OSPI FLASH. OSPI includes two sets of sub-interfaces, namely OSPI0 and OSPI1. Users can choose default GPIO pin or designate required pins through the host computer. OSPI FLASH operation includes clock frequency division, single-line mode configuration, and eight-line mode configuration. After related configurations are set, the host computer can download a designated bin file to OSPI Flash, and with the uploading function, it can upload the OSPI Flash data within a designated range to designated file.

Note: GPIO pin of OSPI configured through the host computer may occupy pins of USART, USB, and SDIO interfaces, so other interfaces can be connected after the pin is reset.

7. Revision history

Table 7-1. Revision history

Revision No.	Description	Date
1.0	Initial release	Jun.14, 2023

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